CLAIMS:

1. An analog-to-digital converter (ADC) for producing coarse digital data based on the analog signals, wherein the ADC comprises:

an integrator coupled to receive the analog signals to produce an integrated output;

a quantizer coupled to receive the integrated output and for producing a digital value coarsely reflecting an amplitude of the integrated output based upon randomly fluctuating reference levels, the quantizer further comprising:

a comparator module for comparing the randomly fluctuating reference levels to the integrated output and for producing the digital value; and

a fluctuating reference level generator for generating the randomly fluctuating reference levels to the comparator module; and

a digital-to-analog converter to convert the digital value to an analog feedback signal produced to the integrator.

2. The ADC of claim 1 wherein the quantizer further includes:

a reference generator for providing a plurality of reference levels; and

a multiplex module for selecting among the plurality of voltage reference levels to produce the randomly fluctuating reference levels based upon a pseudo-random sequence bit stream; and

a pseudo-random sequence bit stream generator for generating the pseudo-random sequence bit stream to the multiplex module.

3. The ADC of claim 2 wherein the plurality of voltage references are produced by a voltage divider having at least two reference levels coupled to each multiplex module within the ADC.

4. The ADC of claim 1 wherein the comparator module further includes:

a plurality of comparators coupled to receive the randomly fluctuating reference levels wherein each of the plurality of comparators produces a binary signal indicating whether the integrated output magnitude exceeds the received randomly fluctuating reference level; and

logic for receiving the binary signal produced by each of the plurality of comparators, the logic producing the digital value wherein the digital value reflects which of the plurality of comparators produced the binary signal as a logic "1" indicating that the integrated output exceeded the received fluctuating reference signal.

5. The ADC of claim 1 wherein the quantizer further includes a plurality of multiplex modules coupled to provide a selected voltage of at least two voltage levels to a corresponding comparator of a plurality of comparators within the comparator module wherein the selected voltage input is the randomly fluctuating reference level to which the integrated output voltage produced by the integrator is compared.

6. The ADC of claim 5 wherein each multiplexer module selects, based upon a pseudo-random sequence of bits produced by a pseudo-random sequence bit stream generator, which of the at least two voltages to provide as an input to a corresponding comparator of the plurality of comparators.

7. A quantizer within a continuous time delta sigma analog-to-digital converter, comprising:

a reference generator further for producing a first number of reference voltage levels for a second number of comparators;

voltage reference selection circuitry for selecting a second number of voltage levels from the first number of reference voltage levels for the second number of comparators;

a pseudo-random sequence bit generator for producing random control signals to the voltage reference selection circuitry wherein the voltage reference selection circuitry selects the second number of voltage levels based on the random control signals; and

comparator circuitry for comparing the selected voltage levels to an input voltage to produce a digital signal having a value reflecting a magnitude of the input voltage.

8. The quantizer of claim 7 wherein at least six reference voltage levels are produced by the reference generator and wherein the voltage selection circuitry selects half of the at least six reference voltage levels for the second number of comparators.

9. An analog-to-digital converter (ADC) for producing coarse digital data based on the analog signals, wherein the ADC comprises:

an integrator coupled to receive the analog signals to produce an integrated output;

a quantizer coupled to receive the integrated output and for producing a digital value coarsely reflecting an amplitude of the integrated output based upon reference levels produced by a reference generator, the quantizer further comprising a comparator module for comparing the reference levels to the integrated output and for producing the digital value;

a digital-to-analog converter to convert the digital value to an analog feedback signal produced to the integrator;

logic for generating a shaped pseudo-random sequence;

current injection circuitry for sinking and sourcing current from and to the feedback signal based upon a logic value of a bit of the shaped pseudo-random sequence.

10. The ADC of claim 10 wherein the logic further includes a pseudo-random bit stream generator.

11. The ADC of claim 10 wherein the pseudo-random bit stream generator includes a linear feedback shift register.

12. The ADC of claim 10 wherein the logic further includes shaping logic for producing shaped pseudo-random sequence based upon an output of the pseudo-random bit stream generator.

13. A method for converting an analog signal to digital, comprising:

receiving an analog signal and a feedback signal;

integrating the analog signal;

quantizing an integrated analog signal;

converting a quantized signal into the feedback signal; and

selecting and adding a dither signal based on a pseudo-random generator bit stream value to one of the integrated analog signal and the feeback signal.

14. The method of claim 13 wherein selecting a dither signal based on a pseudo-random generator bit stream value further includes selecting one of adding a dither voltage to the integrated analog signal or injecting a dither current into the feedback signal.

15. The method of claim 13 wherein injecting a dither current into the feedback signal further includes sinking a dither current from the feedback signal.

16. The method of claim 15 wherein injecting a dither current into the feedback signal includes sourcing a dither current into the feedback signal.

17. The method of claim 14 wherein selecting and adding a dither signal further includes shaping the dither signal as a high pass signal.

18. The method of claim 17 wherein a dither current is injected into a pair of feedback branches in a second order continuous time delta sigma analog to digital converter.

19. The method of claim 14 wherein selecting and adding a dither signal further includes shaping the dither signal as a bandpass shaped dither signal with a selected center frequency.

20. A radio transceiver, comprising:

front end transmitter circuitry for receiving digital data and for converting the digital data to outgoing analog signals, for upconverting the outgoing analog signals to RF signals, and for transmitting the RF signals;

front end receiver circuitry for receiving and down converting RF signals to incoming analog signals at one of an intermediate frequency and a baseband frequency; and

at least one analog-to-digital converter (ADC) coupled to receive one of the outgoing and incoming analog signals (collectively "analog signals"), the ADC for producing coarse digital data based on the analog signals, wherein the ADC comprises:

an integrator coupled to receive the analog signals to produce an integrated output;

a quantizer for producing a digital output having a digital value coarsely reflecting an amplitude of the analog signals based upon randomly fluctuating reference levels, wherein the reference levels fluctuate based on a received pseudo-random sequence bit stream;

a digital-to-analog converter for converting the digital output to a feedback signal that is produced to the integrator;

a random signal generator for producing a pseudo-random sequence bit stream to be added to one of an input of the quantizer or to logic for shaping the noise from the pseudo-random sequence prior to adding it to the feedback signal; and

a digital-to-analog converter to convert the digital output to an analog feedback signal to produce a feedback to the integrator.

21. The radio transceiver of claim 20 wherein the quantizer further includes a plurality of multiplexer modules coupled to provide one of at least two voltage levels as a selected voltage input to a corresponding comparator of the plurality of comparators wherein the selected voltage input is the specified voltage to which the input voltage level is compared.

22. The radio transceiver of claim 20 wherein each multiplexer module selects, based upon the random sequence of bits, which of the at least two voltages to provide as an input to a corresponding comparator of the plurality of comparators.

23. A continuous time delta sigma analog to digital converter (CTΔΣADC), comprising:

means for producing fluctuating reference levels;

means for selecting a subset of the fluctuating reference levels;

means for comparing the subset of fluctuating reference levels to an analog input signal; and

means for producing a digital value coarsely reflecting an amplitude of the analog input signal.

24. The CTΔΣADC of claim 23 wherein the means for comparing further includes a first plurality of comparators, each comparator having a voltage input coupled to a receive an input voltage and a quantizer input coupled to receive a fluctuating comparator reference level.

25. The CTΔΣADC of claim 23 wherein the means for comparing further includes a corresponding plurality of multiplexers, each multiplexer producing the fluctuating comparator reference level to the corresponding comparator based on a reference level selection signal, wherein each of the multiplexers is further coupled to receive at least two comparator reference levels.

26. A continuous time delta sigma analog to digital converter (CTΔΣADC), comprising:

means for producing a shaped noise current source;

means for converting an analog signal to a digital signal;

means for converting the digital signal to analog; and

means for adding the shaped noise current source to an output of the means for converting the digital signal to analog.

27. The CTΔΣADC of claim 26 wherein the shaped noise current source is high pass shaped.

28. The CTΔΣADC of claim 26 wherein the shaped noise current source is band pass shaped.